CLAIMS

We claim:

1. A method comprising:

exposing a semiconductor wafer to a first mask part that is at least partially defective; and,

exposing the semiconductor wafer to a second mask part corresponding to the first mask part and that is at least substantially free from defects or with defects at different locations.

2. The method of claim 1, wherein the first mask part and the second mask part are on a same photomask.

3. The method of claim 1, wherein the first mask part and the second mask part are on different photomasks.

4. The method of claim 1, further comprising exposing the semiconductor wafer to the second mask part a second time.

5. The method of claim 4, further comprising exposing the semiconductor wafer to the second mask part a third time.

6. The method of claim 1, further comprising exposing the semiconductor wafer to the second mask part one or more additional times.

7. The method of claim 1 further comprising exposing the semiconductor wafer to the second, a third and other additional mask parts one or more additional times.

8. The method of claim 1, wherein the first mask part comprises a layout for a semiconductor device that is at least partially defective, and the second mask part comprises a layout for the semiconductor device that is at least substantially free from defects or with defects at different locations.

9. The method of claim 1, wherein exposing the semiconductor wafer to the first mask part and exposing the semiconductor wafer to the second mask part are part of a lithographic semiconductor fabrication process.

10. A semiconductor device fabricated at least in part by performing a method comprising:

exposing a semiconductor wafer on which the device is to be fabricated to a first mask having a layout of the device and that is at least partially defective; and,

exposing the semiconductor wafer to a second mask having the layout of the device and that is at least substantially free from defects or with defects at different locations.

11. The semiconductor device of claim 10, wherein the method further comprises exposing the semiconductor wafer to the second mask a second time.

12. The semiconductor device of claim 9, wherein the method further comprises exposing the semiconductor wafer to the second mask a third time.

13. The semiconductor device of claim 10, wherein the method further comprises exposing the semiconductor wafer to the second mask one or more additional times.

14. The semiconductor device of claim 10, wherein the method further comprises exposing the semiconductor wafer to the second or third or other additional mask one or more additional times.

15. The semiconductor device of claim 10, wherein the layout for each of the first mask and the second mask is only for the device being fabricated.

16. The semiconductor device of claim 10, wherein exposing the semiconductor wafer to the first mask and exposing the semiconductor wafer to the second mask are part of a lithographic semiconductor fabrication process.

17. A semiconductor device fabricated at least in part by performing a method comprising:

exposing a semiconductor wafer on which the device is to be fabricated to a first part of a mask having a layout of the device and that is at least partially defective; and,

exposing the semiconductor wafer to a second part of the mask having the layout of the device and that is at least substantially free from defects or with defects at different locations.

18. The semiconductor device of claim 17, wherein the method further comprises exposing the semiconductor wafer to the second part of the mask a second time.

19. The semiconductor device of claim 18, wherein the method further comprises exposing the semiconductor wafer to the second part of the mask a third time.

20. The semiconductor device of claim 17, wherein the method further comprises exposing the semiconductor wafer to the second part of the mask one or more additional times.

21. The semiconductor device of claim 17, wherein the method further comprises exposing the semiconductor wafer into the second or third or other additional part of the mask one or more additional times.

22. The semiconductor device of claim 17, wherein the mask has a plurality of parts, including the first and the second parts, each having the layout for the device being fabricated.

23. The semiconductor device of claim 17, wherein exposing the semiconductor wafer to the first part of the mask and exposing the semiconductor wafer to the second part of the mask are part of a lithographic semiconductor fabrication process.